In the Claims

Claims 1-70 (cancelled).

Claim 71 (previously presented): A computer system comprising:

a signal source arranged to provide a data signal; and

an inverter coupled with the signal source, configured to invert the data signal and arranged to output the inverted signal; the inverter including:

a structure comprising silicon and germanium;

a first transistor supported by the structure, the first transistor comprising a first gate and a first active region proximate the first gate; the first active region including a first channel region and a pair of first source/drain regions; at least a portion of the first active region being within the structure, the first transistor being a PFET and the first source/drain regions accordingly being p-type doped regions; the first gate being substantially non-overlapping with respect to the first source/drain regions;

an insulative material over at least a portion of the first transistor;

a first layer of semiconductive material over the insulative material;

a second layer of semiconductive material over the first layer, the second layer of semiconductive material physically contacting the first layer of semiconductive material, and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material;

a second transistor over the insulative material, and supported by the first and second layers of semiconductive material, the second transistor comprising a second gate and a pair of second source/drain regions, the second transistor being an NFET and the second source/drain regions accordingly being n-type doped regions; the second source/drain regions extending into the second layer of semiconductive material; the second gate being directly over the first gate; the second gate being substantially non-overlapping with respect to the second source/drain regions;

the first and second gates being electrically connected to one another, and being in electrical connection with the signal source; and

one of the first source/drain regions being electrically connected with one of the second source/drain regions and being in electrical connection with the output.

Claim 72 (previously presented): The computer system of claim 71 wherein the second layer of semiconductive material is a crystalline layer having a relaxed crystalline lattice, and further comprising a strained crystalline lattice layer between the second layer of semiconductive material and the second gate.

Claim 73 (original): The computer system of claim 72 wherein the strained crystalline lattice layer includes silicon.

Claims 74 and 75 (canceled).

Claim 76 (original): The computer system of claim 72 wherein the strained crystalline lattice layer includes silicon and germanium.

Claim 77 (canceled).

Claim 78 (original): The computer system of claim 72 wherein the entirety of the relaxed crystalline lattice is a single crystal.

Claim 79 (original): The computer system of claim 72 wherein the relaxed crystalline lattice is polycrystalline.

Claim 80 (original): The computer system of claim 72 wherein the relaxed crystalline lattice includes Si/Ge.

Claim 81 (original): The computer system of claim 80 wherein the relaxed crystalline lattice comprises from about 10 to about 60 atomic percent germanium.

Claims 82-88 (canceled).

Claim 89 (previously presented): The computer system of claim 72 wherein:

the first channel region is between the first source/drain regions;

the first gate is above the first channel region; and

the width of the first gate with respect to a cross sectional view of the inverter is substantially the same as the width of the first channel region with respect to the cross sectional view.

Claim 90 (previously presented): The computer system of claim 72 wherein the first gate is neither above nor below the first source/drain regions and the second gate is neither above nor below the second source/drain regions.

Claim 91 (new): The computer system of claim 71 wherein the inverter further comprises a p-type doped vertically extending pillar in electrical contact with one of the first source/drain regions and also in electrical contact with the first layer of semiconductive material.

Claim 92 (new): The computer system of claim 71 wherein the inverter further comprises a p-type doped vertically extending pillar in physical contact with one of the first source/drain regions and also in physical contact with the first layer of semiconductive material.

Claim 93 (new): The computer system of claim 92 wherein the first layer of semiconductive material has a bottom surface extending substantially horizontally, and wherein the vertically extending pillar extends substantially perpendicular to the bottom surface.

Claim 94 (new): The computer system of claim 92 wherein the p-type doped vertically extending pillar physically contacts the first layer of semiconductive material at a location directly under one of the second source/drain regions; and wherein the first layer of semiconductive material is p-type doped at the location where the p-type doped vertically extending pillar physically contacts the first layer.

Claim 95 (new): The computer system of claim 94 wherein the p-type doped vertically extending pillar comprises at least two portions which are doped to different concentrations relative to one another.

Claim 96 (new): The computer system of claim 71 wherein the structure comprises a crystalline layer and an entirety of the first channel region is within a single crystal of the structure.

Claim 97 (new): A computer system comprising:

a signal source arranged to provide a data signal; and

an inverter coupled with the signal source, configured to invert the data signal and arranged to output the inverted signal; the inverter including:

a structure comprising silicon and germanium;

a first transistor supported by the structure, the first transistor comprising a first gate and a first active region proximate the first gate; the first active region including a first channel region and a pair of first source/drain regions; at least a portion of the first active region being within the structure, the first transistor being a PFET and the first source/drain regions accordingly being p-type doped regions; the first gate being substantially non-overlapping with respect to the first source/drain regions;

an insulative material over at least a portion of the first transistor;

a first layer of semiconductive material over the insulative material;

a second layer of semiconductive material over the first layer, the second layer of semiconductive material physically contacting the first layer of semiconductive material, and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material;

a second transistor over the insulative material, and supported by the first and second layers of semiconductive material, the second transistor comprising a second gate and a pair of second source/drain regions, the second transistor being an NFET and the second source/drain regions accordingly being n-type doped regions; the second source/drain regions extending into the second layer of semiconductive material; the second gate

being directly over the first gate; the second gate being substantially non-overlapping with respect to the second source/drain regions;

the first and second gates being electrically connected to one another, and being in electrical connection with the signal source;

one of the first source/drain regions being electrically connected with one of the second source/drain regions and being in electrical connection with the output; and

a p-type doped vertically extending pillar in electrical contact with one of the first source/drain regions and also in electrical contact with the first layer of semiconductive material.

Claim 98 (new): A computer system comprising:

a signal source arranged to provide a data signal; and

an inverter coupled with the signal source, configured to invert the data signal and arranged to output the inverted signal; the inverter including:

a structure comprising silicon and germanium;

a first transistor supported by the structure, the first transistor comprising a first gate and a first active region proximate the first gate; the first active region including a first channel region and a pair of first source/drain regions; at least a portion of the first active region being within the structure, the first transistor being a PFET and the first source/drain

regions accordingly being p-type doped regions; the first gate being substantially non-overlapping with respect to the first source/drain regions;

an insulative material over at least a portion of the first transistor;

a first layer of semiconductive material over the insulative material;

a second layer of semiconductive material over the first layer, the second layer of semiconductive material physically contacting the first layer of semiconductive material, and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material;

a second transistor over the insulative material, and supported by the first and second layers of semiconductive material, the second transistor comprising a second gate and a pair of second source/drain regions, the second transistor being an NFET and the second source/drain regions accordingly being n-type doped regions; the second source/drain regions extending into the second layer of semiconductive material; the second gate being directly over the first gate; the second gate being substantially non-overlapping with respect to the second source/drain regions;

the first and second gates being electrically connected to one another, and being in electrical connection with the signal source;

one of the first source/drain regions being electrically connected with one of the second source/drain regions and being in electrical connection with the output;

a p-type doped vertically extending pillar in physical contact with one of the first source/drain regions and also in physical contact with the first layer of semiconductive material.

Claim 99 (new): A computer system comprising:

a signal source arranged to provide a data signal; and

an inverter coupled with the signal source, configured to invert the data signal and arranged to output the inverted signal; the inverter including:

a structure comprising silicon and germanium;

a first transistor supported by the structure, the first transistor comprising a first gate and a first active region proximate the first gate; the first active region including a first channel region and a pair of first source/drain regions; at least a portion of the first active region being within the structure, the first transistor being a PFET and the first source/drain regions accordingly being p-type doped regions; the first gate being substantially non-overlapping with respect to the first source/drain regions;

an insulative material over at least a portion of the first transistor;

a first layer of semiconductive material over the insulative material;

a second layer of semiconductive material over the first layer, the second layer of semiconductive material physically contacting the first layer

of semiconductive material, and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material;

a second transistor over the insulative material, and supported by the first and second layers of semiconductive material, the second transistor comprising a second gate and a pair of second source/drain regions, the second transistor being an NFET and the second source/drain regions accordingly being n-type doped regions; the second source/drain regions extending into the second layer of semiconductive material; the second gate being directly over the first gate; the second gate being substantially non-overlapping with respect to the second source/drain regions;

the first and second gates being electrically connected to one another, and being in electrical connection with the signal source;

one of the first source/drain regions being electrically connected with one of the second source/drain regions and being in electrical connection with the output; and

a p-type doped vertically extending pillar in physical contact with one of the first source/drain regions and also in physical contact with the first layer of semiconductive material at a location directly under one of the second source/drain regions, the first layer of semiconductive material being p-type doped at the location where the p-type doped vertically extending pillar physically contacts the first layer.

Claim 100 (new): A computer system comprising:

a signal source arranged to provide a data signal; and

an inverter coupled with the signal source, configured to invert the data signal and arranged to output the inverted signal; the inverter including:

a structure comprising a crystalline layer including silicon and germanium;

a first transistor supported by the structure, the first transistor comprising a first gate and a first active region proximate the first gate; the first active region including a first channel region and a pair of first source/drain regions; at least a portion of the first active region being within the structure, the first transistor being a PFET and the first source/drain regions accordingly being p-type doped regions; the first gate being substantially non-overlapping with respect to the first source/drain regions; an entirety of the first channel region being within a single crystal of the structure;

an insulative material over at least a portion of the first transistor;

a first layer of semiconductive material over the insulative material;

a second layer of semiconductive material over the first layer, the second layer of semiconductive material physically contacting the first layer of semiconductive material, and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material;

a second transistor over the insulative material, and supported by the first and second layers of semiconductive material, the second transistor comprising a second gate and a pair of second source/drain regions, the second transistor being an NFET and the second source/drain regions accordingly being n-type doped regions; the second source/drain regions extending into the second layer of semiconductive material; the second gate being directly over the first gate; the second gate being substantially non-overlapping with respect to the second source/drain regions;

the first and second gates being electrically connected to one another, and being in electrical connection with the signal source; and

one of the first source/drain regions being electrically connected with one of the second source/drain regions and being in electrical connection with the output.